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10/021,012	12/19/2001	Masahiro Yasukawa	040076.01	9786

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EXAMINER	
QI, ZHI QIANG	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,012	YASUKAWA, MASAHIRO	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/955,461.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12/31/03* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 26, 2003 has been entered.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 is dependent on the claim 1. The claim 1 recites ". . . a silicon nitride film formed as an insulating interlayer between said reflecting electrodes and a metal layer . . .", that means the insulating interlayer between said reflecting electrodes and a metal layer having a silicon nitride film. However, the claim 2 recites ". . . said insulating interlayer between said reflecting electrodes and a metal layer comprising a silicon nitride film and a silicon oxide film . . ." that constitute an indefinite for the insulating interlayer structure. For examination purpose, it is interpreted as the insulating interlayer having a silicon nitride film and a silicon oxide film.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,767,827 (Kobayashi et al) in view of US 5,805,252 (Shimada et al) and US 5,978,056 (Shintani et al).

Claims 1 and 14, Kobayashi discloses (col.4, lines 18–64; Fig.1) that a liquid crystal panel comprising:

- reflecting electrodes (9) formed on a substrate (1), and having a space between adjacent reflecting electrodes;
- a switching element (2,3,4) formed corresponding to each of the reflecting electrode (9);
- a passivation film (11) formed on the reflecting electrodes (9) is a silicon oxide film as a protective film for the pixel transistor on the pixel electrodes;
- insulating films (7a and 7b) (as an insulating interlayer) formed between the reflecting electrode (9) and a capacitance electrode

(20) (the capacitance electrode '20' must be made of a metal, also the data line '8' and the drain electrode '23' must made of metal, and functions as a shielding layer) above the switching element (2,3,4), therefore, the insulating films (7a and 7b) as an insulating interlayer also formed between the reflecting electrode (9) and the switching element (2,3,4) so as to cover the switching elements (2,3,4) except for a connection portion connecting between the reflecting electrode (9) and the switching element (2,3,4).

Kobayashi does not expressly disclose that the insulating film is silicon nitride film, and the metal layer as a light shielding layer shields the incident light to the switching element and disposed under the reflecting electrodes and the space between the adjacent reflecting electrodes so as to cover the switching element .

However, Shimada disclosed (col.1, line 67-col.2, line 1) that an insulating film is made of silicon nitride or silicon oxide, and a dielectric film as an insulating film made of silicon nitride or silicon oxide was common and known in the art. Shimada does not expressly disclose the light shielding. However, Shintani discloses (col.9, line 64 – col.10, 18; Fig.13) that a light shielding layer (51, 52) is disposed under the reflective electrode (8a) and the space between the adjacent reflective electrodes (8a) so as to cover the switching element (5,6,7), and such that prevent multiple reflection of light between the upper surfaces of the light shielding layer and the lower surfaces of the reflective electrodes and the occurrence of photoconductions in the Si substrate is effectively suppressed.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange a silicon nitride film formed as an insulating interlayer and a light shielding layer under the pixel electrodes and the space between the adjacent pixel electrode as claimed in claims 1 and 14 for achieving the insulation and the insulating effect having moisture resistance and suppressing the occurrence of photoconductions in the Si substrate effectively.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi, Shimada and Shintani as applied to claims 1 and 14 above, and further in view of US 5,056,895 (Kahn).

Claim 2, Kobayashi, Shimada and Shintani do not expressly disclose that the insulating interlayer having laminated structure.

However, Kahn discloses (col.4, line 51 – col.6, line 66; Fig.1) that a liquid crystal panel substrate comprising a semiconductor substrate (40) and is then covered with a silicon dioxide dielectric insulating layer (50), and an additional oxide layer (53) covers the first oxide layer, and both of them are between the electrode (70) (composed of Au 'gold', so that must be reflective electrode) and the drain electrode (44) (the drain electrode must be a conductive metal material). Therefore, the insulating interlayer (50,53) has a laminate structure. Kahn also indicates (col.5, lines 40-42) that the composition of oxide layer 50,53,64,68, is well known in the art, and is preferably either SiO_2, or Si_3N_4. Therefore, the insulating layer (53) using silicon nitride film formed on the insulating layer (50) using silicon oxide film would have been obvious, and using

dielectric films having different optical density would have dielectric mirror effect to increase the reflectance.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use laminated insulating films as claimed in claim 2 for increasing the reflectance.

6. Claims 3, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Us 5,510,918 (Matsunaga et al) in view of US 5,056,895 (Kahn).

Claim 3, Matsunaga discloses (col.4, line 12 – col.5, line 32; Figs.1,8) that a liquid crystal display comprising a periphery region of the pixel region on the substrate (SUB1) having gate terminal (GTM) and drain terminal (DTM) (the terminal must be made of metal) and insulating layer (GI), passivation film (PSV1), such that the periphery region having at least insulation interlayers. Matsunage also discloses (col.7, line 62 – col.8, line 20; Fig.8) that a liquid crystal display comprising a passivation film (PSV1) made from silicon nitride film or silicon oxide film formed at the periphery region, and any region having thickness, and the passivation film PSV1 having a high passivation effect is made sufficiently larger than the insulating film GI as to have its peripheral portion passivated as wide as possible. Such that, a passivation film formed on a thickness side of the at least insulating interlayers, and the passivation film having a high passivation effect in the peripheral portion against the humidity or the like, such as moisture resistance.

Matsunaga does not expressly disclose a pixel region having a matrix of reflecting electrodes, and a passivation film having a laminate structure.

However, a reflection type liquid crystal display having reflecting electrode was common and known in the art as using ambient light and reducing power consumption.

Kahn discloses (col.4, line 51 – col.6, line 66; Fig.1) that a liquid crystal panel substrate comprising a semiconductor substrate (40) and is then covered with a silicon dioxide dielectric insulating layer (50), and an additional oxide layer (53) covers the first oxide layer, and both of them are between the electrode (70) (composed of Au 'gold', so that must be reflective electrode) and the drain electrode (44) (the drain elect rode must be a conductive metal material). Therefore, the insulating interlayer (50,53) has a laminate structure. Kahn also indicates (col.5, lines 40-42) that the composition of oxide layer (50,53,64,68) is well known in the art, and is preferably either SiO_2, or Si_3N_4. Therefore, the insulating layer (53) using silicon nitride film formed on the insulating layer (50) using silicon oxide film would have been obvious, and using dielectric films having different optical density would have dielectric mirror effect to increase the reflectance.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use reflecting electrodes and the passivation film (also is an insulating film) as claimed in claim 3 for reducing power consumption and increasing the reflectance.

Claim 8, Matsunaga discloses (Fig.8) that a seal material (SL) formed on the passivation film (PSV1) (silicon nitride film) for sealing with a counter substrate (SUB2).

Claim 9, inherently, the edge section is a scribed region of the substrate to form the periphery region, and that was a common and known in the art for more precisely forming a periphery region making a scribed region on the substrate.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over 5,767,827 (Kobayashi et al) in view of US 5,510,918 (Matsunaga et al).

Claim 4, Kobayashi discloses (col.4, lines 18–64; Fig.1) that a liquid crystal panel comprising:

- reflecting electrodes (9) formed on a substrate (1) and a transistor formed corresponding the each of the reflecting electrodes;
- a drive circuit for scanning the signals formed around the display pixel area (a peripheral circuit arranged in a periphery region of the pixel region on the substrate for supplying signal to the transistors in the pixel region);
- a pssivation film comprising a silicon oxide film (11) formed on the reflecting electrodes (9) in the pixel region.

Kobayashi does not expressly disclose that a second passivation film comprising a silicon nitride film formed at least on a thickness side of the periphery region.

However, Matsunaga discloses (Figs. 7,8) that a passivation film (PSV1) (silicon nitride film) formed on the periphery region (any side region having thickness, so that also is formed on a thickness side of the periphery region), and the passivation film (PSV1) having a high passivation effect for protecting the transistor against humidity.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange a passivation film at least on a thickness side of the periphery region as claimed in claim 4 for achieving humidity resistant.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi and Matsunaga as applied to claim 4 above, and further in view of US 5,805,252 (Shimada et al).

Claim 5, Kobayashi discloses (col.4, lines 18–64; Fig.1) that insulating film (7a, 7b) provided between the reflecting electrode (9) and a capacitance electrode (20) (the capacitance electrode must be made of a metal), so that is an insulating interlayer provided between the reflecting electrode and a metal layer.

Although Kobayashi does not expressly disclose the insulating interlayer is a silicon nitride film, but as an insulating layer made of silicon nitride was common and known in the art as the silicon nitride having insulation property. Such as Shimada discloses (col.1, line 67-col.2, line 1) that an insulating film is made of silicon nitride or silicon oxide, and that would have been at least obvious as using two silicon nitride films would increase the insulating property.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi and Matsunaga as applied to claim 4 above, and further in view of US 5,056,895 (Kahn).

Claim 6, kobayashi and Matsunaga do not expressly disclose the insulating interlayer having a laminate structure.

However, Kahn discloses (col.4, line 51 – col.6, line 66; Fig.1) that a liquid

crystal panel substrate comprising a semiconductor substrate (40) and is then covered with a silicon dioxide dielectric insulating layer (50), and an additional oxide layer (53) covers the first oxide layer, and both of them are between the electrode (70) (composed of Au 'gold', so that must be reflective electrode) and the drain electrode (44) (the drain elect rode must be a conductive metal material). Therefore, the insulating interlayer (50,53) has a laminate structure. Kahn also indicates (col.5, lines 40-42) that the composition of oxide layer (50,53,64,68) is well known in the art, and is preferably either SiO_2, or Si_3N_4. Therefore, the insulating layer (53) using silicon nitride filmed on the insulating layer (50) using silicon oxide film would have been obvious, and using dielectric films having different optical density would have dielectric mirror effect to increase the reflectance.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use laminated insulating films as claimed in claim 6 for increasing the reflectance.

10. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,510,918 (Matsunaga et al) in view of US 5,056,895 (Kahn).

Claim 7, Matsunaga discloses (col.7, line 62 – col.8, line 20; Fig.8) that a liquid crystal display comprising a passivation film (PSV1) made from silicon nitride film formed at the periphery region, i.e., a passivation film formed on the edge region (scribed region on the periphery of the pixel region) of a substrate, and the passivation film having a high passivation effect in the peripheral portion

against the humidity or the like, and the terminal (DTM) connected to the video signal drive circuit, such that the peripheral circuit arranged in the peripheral region of the pixel region and must have metal layer for supplying signal and having insulating layer to insulate the wires.

Although Matsunaga does not expressly disclose a pixel region having reflecting electrodes, but as a reflection type liquid crystal display having reflecting electrode was common and known in the art as using ambient light and reducing power consumption. Matsunaga does not expressly disclose that a first passivation film comprising a first silicon oxide film formed in the pixel region and a second passivation film having a laminated structure. However, Kahn discloses (col.5, lines 35-56; Fig.1) that using the composition of oxide layers (50,53,64,68) is well known in the art, and preferably using silicon oxide or silicon nitride (SiO_2, or Si_3N_4), and such that the electrodes being covered substantially all of the cell area.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange reflecting electrodes in pixel region and using passivation film having a laminate structure as claimed in claim 7 for reducing power consumption and substantially cover the cell area.

Claim 15, using same material for the first and second silicon oxide layers would simplify the manufacturing process, and that would have been at least obvious.

11. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,510,918 (Matsunaga et al) in view of US 5,056,895 (Kahn).

Claim 10, Matsunaga discloses (col.7, line 62 – col.8, line 20; Fig.8) that a liquid crystal display comprising a passivation film (PSV1) made from silicon nitride film formed at the periphery region, i.e., a passivation film formed on the edge region (scribed region on the periphery of the pixel region) of a substrate, and the passivation film having a high passivation effect in the peripheral portion against the humidity or the like.

Although Matsunaga does not expressly disclose a pixel region having reflecting electrodes, but as a reflection type liquid crystal display having reflecting electrode was common and known in the art as using ambient light and reducing power consumption. Matsunaga does not expressly disclose using semiconductor substrate. However, Kahn discloses (col.5, lines 1-8) that semiconductor substrate (40) is suitable for standard integrated circuit processes that are well known in the art, and using such conventional integrated circuit techniques, the cells can be fabricated singly or in multiples on the silicon wafer.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use reflecting electrodes and semiconductor substrate as claimed in claim 10 for reducing power consumption and using the standard processes to fabricate the cells.

Claim 11, Kahn discloses (col.4, line 51 – col.6, line 66; Fig.1) that a liquid crystal panel substrate comprising a semiconductor substrate (40) and is then covered with a silicon dioxide dielectric insulating layer (50), and an additional oxide layer (53) covers the first oxide layer, and both of them are between the electrode (70) (composed of Au 'gold', so that must be reflective

electrode) and the drain electrode (44) (the drain elect rode must be a conductive metal material) Therefore, the insulating interlayer (50,53) has a laminate structure. Kahn also indicates (col.5, lines 40-42) that the composition of oxide layer 50,53,64,68, is well known in the art, and is preferably either SiO_2, or Si_3N_4. Therefore, the insulating layer (53) using silicon nitride film formed on the insulating layer (50) using silicon oxide film would have been obvious, and using dielectric films having different optical density would have dielectric mirror effect to increase the reflectance.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use the passivation film having a laminate structure as claimed in claim 11 for increasing the reflectance.

12. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,510,918 (Matsunaga et al) in view of US 5,767,827 (Kobayashi et al).

Claim 12, Matsunaga discloses (col.7, line 62 – col.8, line 20; Fig.8) that a liquid crystal display comprising two substrates (SUB 1, SUB2); a liquid crystal (LC) therebetween; a seal material (SL) seeing the two substrates; and a passivation film (PSV1) made from silicon nitride film formed at the periphery region (scribed region formed on the peripheral pf the pixel region), and the passivation film having a high passivation effect in the peripheral portion against the humidity or the like.

Matsunaga does not expressly disclose a pixel region having reflecting electrodes.

However, Kobayashi discloses (Fig.1) that the reflecting electrodes (9) formed in the pixel region, and a reflection type liquid crystal display having reflecting electrode was common and known in the art as using ambient light would reduce the power consumption.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange reflecting electrodes in pixel for reducing power consumption.

Claim 13, Matsunage does not expressly disclose that using first passivation film and second passivation film, and second passivation film formed on the reflecting electrodes.

However, Kobayashi discloses (Fig.1) that the passivation layer (11) formed on the reflecting electrodes (9) and having insulating films (7a,7b) functions as another passivation layer, such that the switching element would obtain more protection.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to arrange a second passivation layer on the reflecting electrode as claimed in claim 13 for obtaining more protection for the switching elements.

Response to Arguments

13. Applicant's arguments filed on Aug.26, 2003 have been fully considered but they are not persuasive.

Applicant's arguments are as follows:

1) The references do not disclose that a silicon nitride film as an insulating interlayer between the reflecting electrodes and a metal layer above the switching element thereunder, wherein the metal layer shields incident light to the switching element.

2) The references do not disclose that a light shielding layer disposed under the reflecting electrodes and the space between adjacent reflecting electrodes so as to cover the switching elements.

3) The references do not disclose that a passivatiion film formed by a silicon nitride film and formed on the scribed region (formed on the peripheral of the pixel region) of the semiconductor substrate.

Examiner's responses to Applicant's arguments are as follows:

1) The reference Kobayashi discloses (col.4, lines 18–64; Fig.1) that insulating films (7a and 7b) (as an insulating interlayer) formed between the reflecting electrode (9) and a capacitance electrode (20) (the capacitance electrode '20' must be made of a metal, also the data line '8' and the drain electrode '23' must made of metal, and functions as a shielding layer) above the switching element (2,3,4), therefore, the metal layer also functions as a light shielding layer to shields the incident light, so as to cover the switching elements (2,3,4).

2) The reference Shintani discloses (col.9, line 64 – col.10, 18; Fig.13) that a light shielding layer (51, 52) is disposed under the reflective electrode (8a) and the space between the adjacent reflective electrodes (8a) so as to cover the switching element (5,6,7).

3) The reference Matsunaga discloses (Figs. 7,8) that a passivation film (PSV1) made from silicon nitride film formed on the periphery region (also is formed on a side of edge sections of the periphery region, and any side edge can be a side edge), and the passivation film (PSV1) having a high passivation effect for protecting the transistor against humidity.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299.

16. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
February 9, 2004

TOAN TON
PRIMARY EXAMINER